Design of an 10 kVA-45 A automatic static transfer switch module

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Abstract

Uninterruptible Power Supplies (UPS's) are designed to provide emergency power when the main power source fails. To avoid this impact and to protect effectively the loads, one solution is to provide a redundant loading system using a dual power energy source other than the UPS to achieve an automatic static transfer when necessary. In this work, an additional module has been designed and connected between a critical load and the output of two independent UPS systems; if primary UPS fails, the module automatically transfers the load to the other one with a minimum transfer switching time.
The results presented demonstrate a transfer switch time below 3 ms, compared to commercial products of 4 to 6 ms.

1 Introduction

The electric power is supplied to users with various uncontrollable factors that can affect their reliability and quality for any commercial systems. For example, an Uninterruptible Power Supply (UPS) can fail due to the depletion of its batteries, harmonics from the electrical network or internal failure among other causes [1]. According to literature, projects using additional control to start external power generator have higher transfer times than 3 minutes [2]. A solution for reducing the transfer time is the use of static transfer switches (STS) that have transfer times less than 30 *m*s. In order to lower transfer time, the use of power semiconductors devices, like thyristors, is needed for their rapid and safe transfer capabilities [3]. Another solution would be using modules with electromechanical automatic transfer (EMTS); however, they have problems with the electromechanical contacts elements that stick to its base due to the heat energy transfer. One more solution is to use the technique of switching operation to an Automatic Static Transfer Switch module (ATS-M) with semiconductors components that will give a higher speed response and allow a quick transfer before having failover or disturbances [4]. Current technology is using faster electronic devices within more complex systems; however, they are more sensitive to electrical disturbances; for that reason loss of information can be caused. Power requirements for critical loads differ by types and manufacturers and today's problems for IT teams are the power supply variation tolerances, which are extremely important when setting protection system boundaries [5]. The 5 main power requirements are the following:

1. Voltage regulation in permanent state (± 5%).
2. Maximum transient condition (+15% or -18% of the rated voltage) with a maximum response time of 0.5 second.
3. Maximum frequency adjustment (± 0.6 Hz).
4. Maximum THD (5%)
5. Maximum unbalance voltage between phases (2.5%).

Figure 1 determinates how important is to limit the transfer switching time, as it shows the waveform of the input voltage, input current and output voltage of a VDC power supply [6]. When the AC input voltage is interrupted, the output voltage fed the load at full capacity during an interval time of 18 milliseconds (for this case) before collapsing completely. This short time gives the opportunity to develop a redundant module to be able to transfer the load to another selected power line.

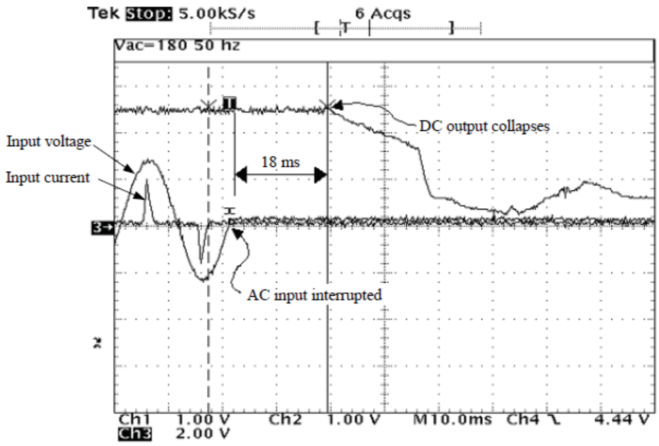


Figure 1: Power supply ride-through [6]

Figure 2 shows the specifications of the international standard IEC 62040-3 [7], where the limits of the magnitude and duration of the voltage disturbances standards are defined. Having the voltage variations expressed in percentages, from +10% to -20% of the nominal value, give design flexibility in for the ATS-M to be developed, because the output voltage varies within a range that does not affect the load operation of the system.
The ATS-M module designed is able to transfer the load to another AC power source in a faster manner so that there is no power loss. This happens when the primary source fails;

the detection of this failure activates and transfers the load to another AC source from two selected power distribution sources.

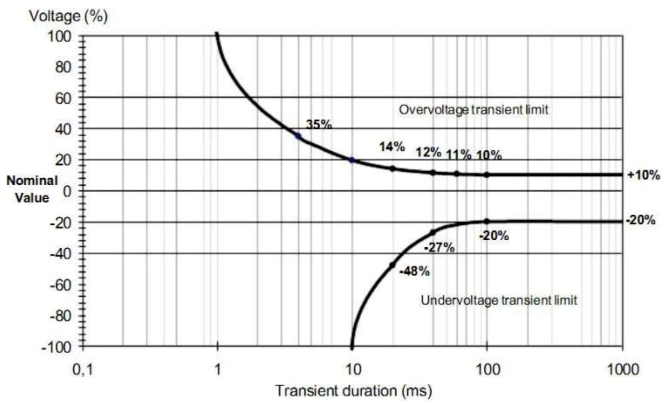


Figure 2: Output dynamic performance classification 3 [7]

2 Design consideration

To have a reliable system, it is needed a 3 way mode design approach [8]:

1. Normal mode: under normal circumstances the automatic transfer panel (ATT) verifies that the main voltage and load are connected to the main network.
2. Power failure mode: when the main line voltage fails or drops to less than a reference value, the system automatically starts the generator and then switches the load.
3. Main energy source return mode: when the main power source returns, the ATT samples and checks that the voltage is adequate to then transfer the load to its main line.

Most of the commercial designs reviewed are using static contactors to realize the load transfer; yet, their response is quiet slow. For this design, the contactors and relays have been replaced by thyristors for their fast response and switching capacity. Thus, the operating principle of the ATS-M is based on the switching techniques of the thyristors, which allow us having a quick load transfer when failures and disturbances occur from the main power source or power line. Transistors generally have better performance at high frequencies because they have higher speed and lower losses. Additionally to simple transistors, thyristors have lower conduction losses in the "on" state and greater current handling.

Figure 3, shows the block diagram of the developed ATS-M where line 1 and line 2 are the two power electrical sources that feed the load; by default line 1 is the main power source.

In order to prevent that the module does not turn-off, it will be fed with two energy sources. The power block is fully isolated from the control block; this is achieved with the isolation of the transformer block and an optocoupler circuit. Then, the microcontroller is responsible for receiving the I/O signals from the sensors and sending the trigger signal to activate the power circuit. The ATS-M has a control unit that monitors the voltage and the frequency quality of both sources. This unit detects any disturbance or system breakdown by sampling and monitoring them. When a failure or a lack of energy superior to the percentage allowed of the nominal value is detected, an alarm immediately sends a signal to the microcontroller to transfer the load to the other source and will generate the signal pulse to trigger the thyristor of the module.

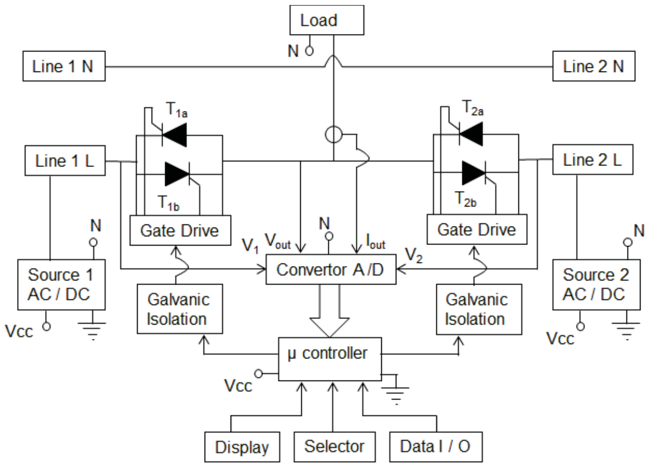


Figure 3: Block diagram of the system

The ATS-M is designed for an intensity work regime of 45 A, a tension of 220 Vac L-N ± 10%, a frequency of 60 Hz and to sustain a power of 10 kVA.

All the system units, such as the power stage, the control system and others have been carefully designed. Each values of the component have been calculated and simulated in OrCAD PSpice to secure its good performance while implemented in its circuitry. For example, to be able to satisfy the high handling currents, a 56 A semipack thyristor (IRKT-56-12) was selected. The design has been optimized several times for the system gate drive, the galvanic isolation, and the modify zero crossing and census technique due to the lack of performance of the transfer time function. Each time a modification was made, simulations were realized to ensure the operation of the module. In figure 4, it is shown the final implemented ATS-M.

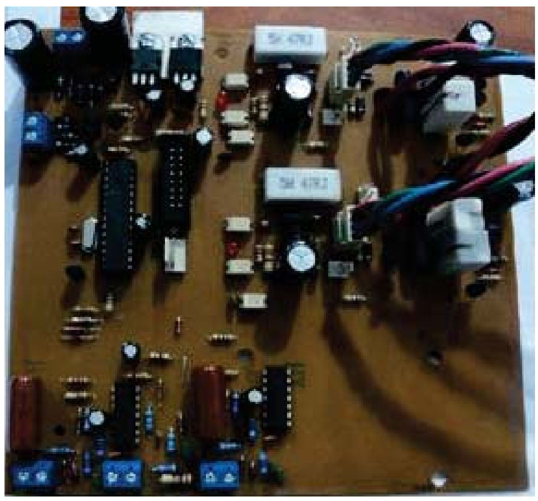


Figure 4: Final ATS-M implementation

3 Results and Discussion

It is important to understand that the purpose of this design and analysis is to compare the differences in time switching between the prototype developed and the available commercial products. As mentioned before, each stages of the design have been carefully revised with acceptable failure rate; however, associating all the circuitry together the results obtained of the transfer time were not good enough, compared to the commercial products existing in the market, until the last version of the design. Preliminary results concluded that the initial release transfer times obtained were way over the 16.6 ms (frequency of 60Hz) of the complete wave cycle. Critical loads were disrupted and caused unexpected functioning problem to the systems. Learning from those failures and to get faster response transfer time and improve the design, various modifications have been realized in both the hardware and software. Figure 5 resumes the transfer time of the various trials realized during the design, implementation, and trial process of the ATS-M.

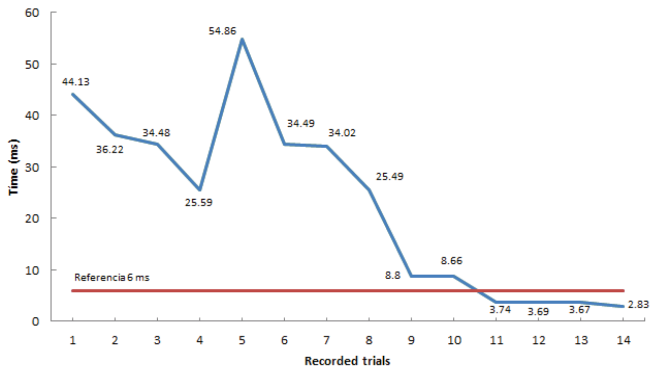
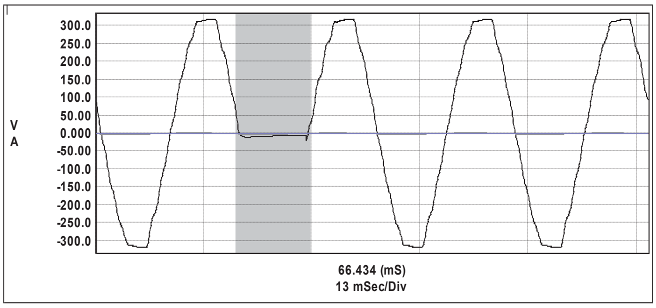
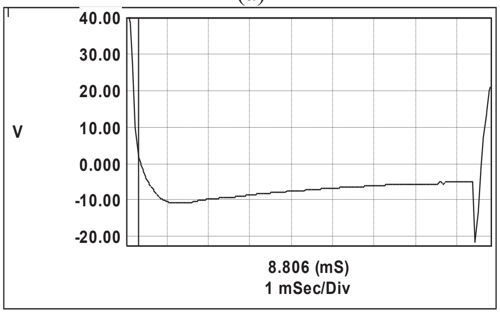


Figure 5: Recorded transfer time of the ATS-M

First, changes in the hardware have been made in the zero crossing census circuit because it was monitoring two power supplies and two lines at the same time. The zero crossing is also essential to control the SCR, it is for this reason it was removed from the output and placed in return to a zero crossing that counted only the input line 1; the same changes have been realized in line 2. With these changes, the time transfer improved a little; however, they were still over the 16 ms cycle mark. It has been noticed that a low current was applied to the SCR trigger hence this problem was then reformulated by changing the pulse width and increasing latching current (Ih) of the semiconductor component.
Then, changes in the control algorithm have been made to ensure signal sampling every half cycle (8.33 ms) as shown in figure 6. Also, the SCR trigger current was increased by the mean of an algorithm to fire the thyristor and drive it properly. Finally, it was chosen to change the switching technique from zero crossing to a constant census technique to have time transfer below the half cycle wave of 8.33 ms and to ensure continuity in the functioning of the critical loads.
Overall, the changes made initially were to obtain transfer time equal to the half wave cycle of 8 ms and a stable system.



(a)

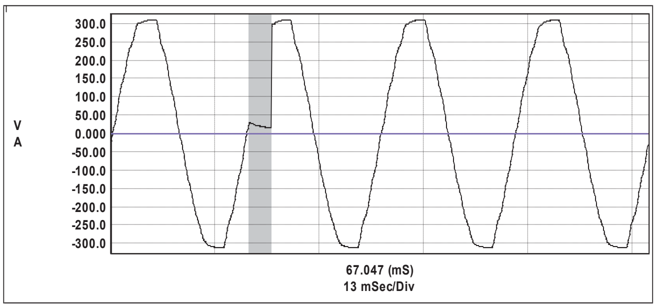


(b)

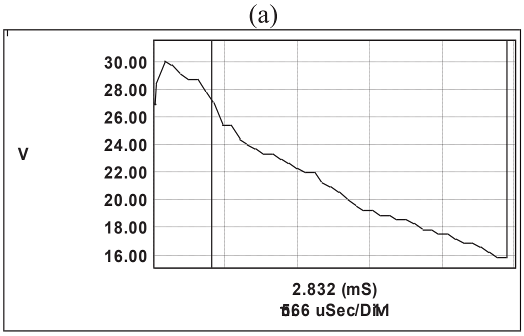
Figure 6: Results of the system with the use of the modify zero crossing technique (a) waveform, (b) time transfer

Brand/Model	*Transfer time*	*Reference*
ATS-M (10kVA-45A)	< 3 ms	This work
Eaton STS 16 (16A)	6 ms	[9]
Libert STS (16A)	< 6 ms	[10]
Libert HiSwitch2 3 poles (50A)	< 4.17 ms (1/4 cycle)	[11]

Table 1: Transfer time comparison of various models



(a)



(b)

Figure 7: ATS-M fastest transfer time results (a) waveform, (b) time transfer

To be able to compete with commercial products (see table 1), it was necessary to shorten the transfer time as much as possible. The use of the sampling technique was applied to process the waveform of the supply line in a continuous manner to detect an absence of the main signal line and also to guarantee a short transfer time. It is vital that the sensing starts every time after each zero crossing pulse in order to perform a synchronously signal sampling. For the first trials, it has been designed a simple algorithm for sampling 10 times the signal to be processed and compared it to the reference. The technique of census sampling helps improving the time transfer and the handling the main source with a constant census, all that aiming to make an instantaneous transfer of the load. Finally, the results obtained show a stable transfer time around 3.6 ms (figure 5, trials 11, 12, and 13) with a shortest transfer time recorded at 2.8 ms (figure 7).

4 Conclusion

The product developed is a redundant transfer system that can be connected in parallel to any UPS system or main power line. The ATS-M features benefits such as, improving reliability and increasing operational safety by reducing the risk of data loss. The system is feed through two independent power sources than can be easily connected to the module and if one power soured fails the transfer will be realized automatically in a rapid manner. The initial trials results were poor; however, they have helped in locating issues in the hardware, software and control scheme of the system. Meanwhile the use of the applied sampling technique, the transferring time has been improved in an effective manner due to the determination of the exact moment when no electrical power was in the main line. Finally, the ATS-M module developed shows better and reliable time transfer, around 3 ms and having a fastest transfer time of 2.8 ms, than commercial products offered by competitors with time within the range from 4 to 6 ms and can still be improved.

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